Fabrication and Properties of *n*Si-*p*CdTe Heterojunctions

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Abstract—nSi-pCdTe heterostructures have been produced by growing a pCdTe layer on an nSi substrate using thermal evaporation in vacuum at a residual pressure of 10^{-3} Pa. We have studied the elemental concentration depth profiles across the pCdTe layer and obtained current—voltage curves and spectral characteristics of the nSi-pCdTe heterostructures.

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INTRODUCTION

Recent years have seen particular research interest in the fabrication of heterojunctions between CdTe and Si because heterostructures based on these materials can offer an alternative approach to solar-to-electrical energy conversion. Such heterojunctions combine the capabilities of silicon solar cells and advantages of cadmium telluride. However, high-quality CdTe-Si heterojunctions are difficult to produce because the lattice parameters of CdTe and Si differ by 15%, which leads to the formation of a high density of surface defects at Si/CdTe interfaces. Nevertheless, recent work has demonstrated the feasibility of producing high-quality CdTe-Si heterojunctions with a low density of surface defects through the formation of an intermediate transition layer, which acts as a buffer in an nSi-pCdTe heterostructure. Note that the intermediate layer should consist of a solid solution ensuring a smooth variation in lattice parameter.

The objectives of this work were to grow compositionally graded CdTe layers on Si substrates, determine the composition of the layers as a function of their thickness, and obtain current-voltage and spectral characteristics of an nSi-pCdTe heterostructure.

It is known that thin CdTe films on various substrates can be grown by a variety of techniques [1, 2]. In recent years, such films are typically produced by thermal deposition in vacuum, that is, by vapor phase growth [3]. In this work, CdTe layers were grown by this method, because it allows one to obtain a variety of fast-response photosensitive structures. Moreover, it offers the possibility of effectively controlling the deposition process to obtain compositionally graded films. For example, Nuriyev et al. [4] investigated the effect of compensation with an additional Te vapor source during the growth process on the surface morphology of CdTe films produced by vacuum sputter deposition. Their results demonstrate that, adjusting the main and compensating source temperatures, one can obtain both n- and p-type CdTe films.

EXPERIMENTAL PROCEDURE AND RESULTS

All heterostructures studied by us were produced via thermal evaporation of CdTe powders. CdTe was slowly evaporated as described elsewhere [5] in a quasi-closed vacuum system at a residual pressure of 10^{-3} Pa. As substrates, we used silicon wafers 300-350 µm in thickness, cut in the (001) and (111) planes from single-crystal n-type silicon ingots with a resistivity $\rho \approx 5-10 \ \Omega$ cm. The Si substrates were prepared (lapped and polished) under plant conditions in accordance with a Russian Federation State Standard. At the same time, contamination on the surface of the silicon wafers due to prolonged storage was removed by an alkaline etchant: aqueous 5% KOH solution. The etching time was 8–10 min. Next, given that KOH is difficult to remove from the surface, the substrates were thoroughly rinsed by a displacement method [6] in two steps. First, the substrates were rinsed in running distilled water for 8–10 min. After that, they were rinsed in deionized water (~20 M Ω) for 3–5 min. Next, the substrates were placed in an infrared drying oven for 15–20 min.



Fig. 1. Micrograph of the film surface.

Most (70–80%) of the samples produced on the substrates cleaned as described above were similar in properties (photosensitivity and shape of current–voltage (I-V) curves). For 20–30% of the samples, deviations of their main parameters were as large as 50–80%.

Microstructural examination showed that the crystallite size in the films strongly depended on process conditions, primarily on the deposition time and substrate temperature. In our film growth runs, the temperature in the crucible containing the CdTe source was varied in the range $t_{source} \approx 800-850^{\circ}$ C and the substrate (nSi) temperature was maintained in the range $t_s \approx 250-270^{\circ}$ C. In addition, to ensure reproducibility of properties, we used a baffle to control the CdTe deposition time, which ensured that films grown in different runs were identical in thickness.

The surface of the CdTe films was examined on an MII-4 optical microscope. The CdTe films were shown to consist of densely packed crystallites (grains) with a rough surface similar to texture (Fig. 1).

In addition, we investigated elemental concentration depth profiles across a CdTe layer with an accuracy of $\pm 2\%$ using a JEOL JXA-8900 electron probe microanalysis system (data acquisition conditions: V=20 kV, I = 10 nA; natural Cd, Te, and Si standards; synthetic FeS standard for S) (Fig. 2). X-ray spectroscopy results are presented in Fig. 3. It is seen in Figs. 2 and 3 that, on the surface of the *n*Si substrate (vertical line 2), the amount of Si exceeds that of CdTe. As the film grows, the amount of Si gradually decreases, and that of CdTe increases. Finally, after line 1 the amount of Si drops to almost a minimum, and the amount of CdTe reaches the maximum level. It is also seen in Fig. 3 that cadmium and tellurium secondary electron emission from the surface of the layers has the highest intensity; that is, the surface layer of the films consists predominantly of CdTe.



Fig. 2. Elemental concentration depth profiles across a heterostructure.

It is known that, to produce a heterojunction with a low density of surface states, the mismatch should be within 7% [7]. However, capacitance–voltage measurements on the interface between a pCdTe layer and nSi substrate showed that the density of surface states was lower than was expected at the beginning of the experiment.

The nSi-pCdTe heterostructures produced in this study were characterized by current-voltage (*I*-*V*) measurements. To this end, electrical contacts were made by vacuum deposition of indium: continuous contacts to the Si substrate and point contacts with an area of ~1 mm² to the *p*CdTe layer. As seen in Fig. 4, the *I*-*V* curve thus obtained has a typical form corresponding to a diode structure.

In addition, we studied spectral characteristics of the nSi-pCdTe structures (Fig. 5). The spectral dependence of photosensitivity was measured at room temperature using a 3MP-3 monochromator. As a



Fig. 3. Distribution of chemical elements over the surface of the layers according to X-ray spectroscopy results.

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Fig. 4. I-V curve of the nSi-pCdTe heterostructure.



Fig. 5. Spectral characteristic of the *n*Si–*p*CdTe heterostructure.

light source, we used a DKSSh-1000 xenon lamp, operating at the minimum possible power. It has a continuous spectrum in the ultraviolet and visible spectral regions. It is seen in Fig. 5 that the descending part of the longer wavelength peak corresponds to silicon, whereas the descending part of the shorter wavelength peak corresponds to cadmium telluride. The intermediate region of the spectral dependence corresponds to the compositionally graded layer formed between the silicon and cadmium telluride.

CONCLUSIONS

We have demonstrated the feasibility of producing compositionally graded CdTe layers on Si substrates, that is, high-quality heterojunctions between CdTe and Si for use as solar cells.

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